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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/938,614	08/27/2001	Hiroshi Kageyama	A8319.0004/P004	2342
24998	7590	05/05/2004	EXAMINER	
DICKSTEIN SHAPIRO MORIN & OSHINSKY LLP 2101 L STREET NW WASHINGTON, DC 20037-1526			SHAPIRO, LEONID	
			ART UNIT	PAPER NUMBER
			2673	14

DATE MAILED: 05/05/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/938,614

Applicant(s)

KAGEYAMA ET AL.

Examiner

Leonid Shapiro

Art Unit

2673

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 12 February 2004.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-52 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-52 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 27 August 2001 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date: _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____

Drawings

1. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the newly introduced limitation of claims 1-4: "or by connecting two output terminals of plurality of **signal lines** to one of the **signal lines** together" must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Specification

2. The specification is objected to as failing to provide proper antecedent basis for the claimed subject matter. See 37 CFR 1.75(d)(1) and MPEP § 608.01(o). Correction of the following is required: the newly introduced limitation of claims 1-4: "or by connecting two output terminals of plurality of **signal lines** to one of the **signal lines** together" are not shown in the originally filed Specification.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. Claims 1-16, 25-44 and 49-52 are rejected under 35 U.S.C. 103(a) as being unpatentable over Proebsting (US Patent No. 5,952,948) in view Akiyama et al. (US Patent No. 6,201,523 B1) and Minami et al. (US Patent No. 5,454,013).

As to claim 1, Proebsting teaches a drive circuit, comprising: a plurality of digital-to-analog conversion circuit (See Fig. 1, items 106-1 to 106-n, See Col. 1, lines 38-49) each of which selects one of difference reference voltages (See Fig. 5, items 404-409, Col. 4, Lines 1-30) corresponding to a digital gradation signal (See Fig. 4, item 410, Col. 4, Lines 30-34); and wherein the digital-to analog conversion circuit between the selected reference voltage and the output terminal of the digital-to analog conversion circuit includes a variable resistor circuit with a resistance value corresponding to a digital gradation signal lines (See Fig. 4-5, items 404,406,408,410, from Col. 4, Line 1 to Col.5, Line 20).

Proebsting does not teach a sampling circuit which connects each output terminal of two of the digital-to-analog conversion circuit to signal lines and wherein the sampling circuit outputs a predetermined voltage by connecting an output voltage terminal of the plurality of digital-to-analog conversion circuits to one of signal lines.

Akiyama et al. teaches a sampling circuit which connects each output terminal of two of the digital-to-analog conversion circuit to signal lines (See Fig. 8, items 113, 123, Col. 9, Lines 26-36); wherein the sampling circuit outputs a predetermined voltage by connecting an output voltage terminal of the plurality of digital-to-analog conversion circuits to one of signal lines (See Fig. 8, items 113, 123, Col. 9, Lines 26-36).

It would have been obvious to one of ordinary skill in the art at the time of invention to add a sampling circuit as shown by Akiyama et al. to the Proebsting apparatus in order to satisfy the need for an LCD column driver circuit that consumes less power and area.

Proebsting and Akiyama et al. do not show a sampling circuit which connects each output terminal of two of the digital-to-analog conversion circuit to signal lines selectively.

Minami et al. teaches a sampling circuit which connects each output terminal of two of the digital-to-analog conversion circuit to signal lines selectively (See Fig. 4, items 16-17 and 20, Col. 7, Lines 42-67).

It would have been obvious to one of ordinary skill in the art at the time of invention to switch each output terminal to signal lines selectively as shown by Minami et al. in the Proebsting and Akiyama et al. apparatus in order to satisfy the need for an LCD column driver circuit that consumes less power and area.

As to claim 2, Proebsting teaches a drive circuit, comprising: a plurality of digital-to-analog conversion circuit (See Fig. 1, items 106-1 to 106-n, See Col. 1, lines 38-49) each of which selects one of difference reference voltages (See Fig. 5, items 404-409, Col. 4, Lines 1-30) corresponding to a digital gradation signal (See Fig. 4, item 410, Col. 4, Lines 30-34; a plurality of switching element groups including a plurality of switching elements which are connected to each other in parallel, wherein each of which has a difference resistance value in active, connects to a corresponding output terminal of the

digital-to-analog conversion circuit and is controlled according to a digital gradation signal (See Fig. 4-5, items 404,406,408,410, from Col. 4, Line 1 to Col.5, Line 20).

Proebsting does not teach a sampling circuit which connects each output terminal of two of the digital-to-analog conversion circuit to signal lines and wherein the sampling circuit outputs a predetermined voltage by connecting an output voltage terminal of the plurality of digital-to-analog conversion circuits to one of signal lines.

Akiyama et al. teaches a sampling circuit which connects each output terminal of two of the digital-to-analog conversion circuit to signal lines (See Fig. 8, items 113, 123, Col. 9, Lines 26-36); wherein the sampling circuit outputs a predetermined voltage by connecting an output voltage terminal of the plurality of digital-to-analog conversion circuits to one of signal lines (See Fig. 8, items 113, 123, Col. 9, Lines 26-36).

It would have been obvious to one of ordinary skill in the art at the time of invention to add a sampling circuit as shown by Akiyama et al. to the Proebsting apparatus in order to satisfy the need for an LCD column driver circuit that consumes less power and area.

Proebsting and Akiyama et al. do not show a sampling circuit which connects each output terminal of two of the digital-to-analog conversion circuit to signal lines selectively.

Minami et al. teaches a sampling circuit which connects each output terminal of two of the digital-to-analog conversion circuit to signal lines selectively (See Fig. 4, items 16-17 and 20, Col. 7, Lines 42-67).

It would have been obvious to one of ordinary skill in the art at the time of invention to switch each output terminal to signal lines selectively as shown by Minami et al. in the Proebsting and Akiyama et al. apparatus in order to satisfy the need for an LCD column driver circuit that consumes less power and area.

As to claim 3, Proebsting teaches a drive circuit, comprising: a plurality of digital-to-analog conversion circuit (See Fig. 1, items 106-1 to 106-n, See Col. 1, lines 38-49) each of which connects one of difference reference voltages (See Fig. 5, items 404-409, Col. 4, Lines 1-30) corresponding to a digital gradation signal (See Fig. 4, item 410, Col. 4, Lines 30-34; wherein each output terminal of the digital-to analog conversion circuits connects to a corresponding variable resistor circuit with a resistance value corresponding to a digital gradation circuit (See Fig. 4-5, items 404,406,408,410, from Col. 4, Line 1 to Col.5, Line 20).

Proebsting does not teach a sampling circuit which connects each output terminal of two of a plurality of variable resistor circuits to one of a plurality to signal lines and wherein the sampling circuit outputs a predetermined voltage by connecting an output voltage terminal of the plurality of digital-to-analog conversion circuits to one of signal lines.

Akiyama et al. teaches a sampling circuit which connects each output terminal of two of the digital-to-analog conversion circuit to signal lines (See Fig. 8, items 113, 123, Col. 9, Lines 26-36); wherein the sampling circuit outputs a predetermined voltage by connecting an output voltage terminal of the plurality of digital-to-analog conversion circuits to one of signal lines (See Fig. 8, items 113, 123, Col. 9, Lines 26-36).

It would have been obvious to one of ordinary skill in the art at the time of invention to add a sampling circuit as shown by Akiyama et al. to the Proebsting apparatus in order to satisfy the need for an LCD column driver circuit that consumes less power and area.

Proebsting and Akiyama et al. do not show a sampling circuit which connects each output terminal of two of plurality of variable resistor circuits to one of plurality signal lines selectively.

Minami et al. teaches a sampling circuit which connects each output terminal of two of the digital-to-analog conversion circuit to signal lines selectively (See Fig. 4, items 16-17 and 20, Col. 7, Lines 42-67).

It would have been obvious to one of ordinary skill in the art at the time of invention to switch each output terminal to signal lines selectively as shown by Minami et al. in the Proebsting and Akiyama et al. apparatus in order to satisfy the need for an LCD column driver circuit that consumes less power and area.

As to claim 4, Proebsting teaches a drive circuit, comprising: a plurality of digital-to-analog conversion circuit (See Fig. 1, items 106-1 to 106-n, See Col. 1, lines 38-49) each of which outputs an analog signal (See Fig. 5, items 404-409, Col. 4, Lines 1-30) corresponding to a digital gradation signal (See Fig. 4, item 410, Col. 4, Lines 30-34; and wherein each output terminal of the digital-to analog conversion circuit connects to a corresponding variable resistor circuit with a resistance value corresponding to a digital gradation signal lines (See Fig. 4-5, items 404,406,408,410, from Col. 4, Line 1 to Col.5, Line 20).

Proebsting does not teach a sampling circuit which connects each output terminal of two of variable resistor circuits to a corresponding one of a plurality of signal lines.

Akiyama et al. teaches a sampling circuit which connects each output terminal of two of variable resistor circuits to a corresponding one of a plurality of signal lines (See Fig. 8, items 113, 123, Col. 9, Lines 26-36); wherein the sampling circuit outputs a predetermined voltage by connecting an output voltage terminal of the plurality of digital-to-analog conversion circuits to one of signal lines (See Fig. 8, items 113, 123, Col. 9, Lines 26-36).

It would have been obvious to one of ordinary skill in the art at the time of invention to add a sampling circuit as shown by Akiyama et al. to the Proebsting apparatus in order to satisfy the need for an LCD column driver circuit that consumes less power and area.

Proebsting and Akiyama et al. do not show a sampling circuit which connects each output terminal of two of a plurality of variable resistor circuits to signal lines selectively.

Minami et al. teaches a sampling circuit which connects each output terminal of two of the digital-to-analog conversion circuit to signal lines selectively (See Fig. 4, items 16-17 and 20, Col. 7, Lines 42-67).

It would have been obvious to one of ordinary skill in the art at the time of invention to switch each output terminal to signal lines selectively as shown by Minami

et al. in the Proebsting and Akiyama et al. apparatus in order to satisfy the need for an LCD column driver circuit that consumes less power and area.

As to claims 5-8, Proebsting teaches switching elements which conduct according to gradation signal as the resistors values corresponding to gradation circuit and resistance elements, connected in series with each other, as the resistors with resistance values corresponding to gradation signal (See Fig. 4-5, items 404,406,408,410, in description from Col. 4, Line 1 to Col.5, Line 20).

As to claims 9-12, Proebsting, Akiyama et al. and Minami et al. teach all limitations reflected in rejections of claims 1-4. The only difference between claims 1-4 and 9-12 positive and negative circuits.

Akiyama et al. teaches to generate negative and positive polarity D/A converters, and a switching block having plurality of switching circuits for receiving the negative and positive polarity analog video signals (See Figs. 8, 10, items 111, 121, 113, 123, from Col. 9, Line 3 to Col. 10, Line 15).

It would have been obvious to one of ordinary skill in the art at the time of invention to generate negative and positive polarity D/A converters, and a switching block having plurality of switching circuits for receiving the negative and positive polarity analog video signals as shown by Akiyama et al. in the Proebsting apparatus to generate positive and negative analog driving signals in order to satisfy the need for an LCD column driver circuit that consumes less power and area.

As to claims 13-16, Proebsting teaches switching elements which conduct according to gradation signal as the resistors values corresponding to gradation circuit

and resistance elements, connected in series with each other, as the resistors with resistance values corresponding to gradation signal (See Fig. 4-5, items 404,406,408,410, in description from Col. 4, Line 1 to Col.5, Line 20).

As to claims 25-32, 49-52, Proebsting teaching plurality of references voltages are fewer in numbers than the gradations of displayed images (See Figs. 3-5, items 300,302,206i, 400, 402, in description See from Col. 3, line 66 to Col. 4, Line9 and Lines 49-58).

As to claims 33-44, Proebsting teaching an image display apparatus with a drive circuit, wherein a plurality of signal lines for transmitting image signals and a plurality of scanning lines for transmitting scanning signals are formed in a matrix-like fashion in an image display area of a substrate, an lector-optical conversion element or liquid crystal which changes its light transmittance or emission intensity to an electrical signal is placed near each intersection of the signal lines and scanning lines or liquid crystals are sandwiched between substrate and another substrate, signal lines are connected to drive circuit, and scanning line connected to a scanning circuit (See Fig.1, items 102-108, in description See Col. 1, Lines 5-65).

4. Claims 17-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Proebsting, Akiyama et al. and Minami et al. as applied to claim 2, 4, 10, 12 above, and further in view of Jeong (US Patent No. 6, 335, 721 B1).

As to claims 17-18, Proebsting, Akiyama et al. and Minami et al. do not show among the groups of the switching elements belonging to sampling circuit, a pair of

switching elements connected to the same signal line conduct simultaneously in response to signal line selection signal.

Jeong teaches among the groups of the switching elements belonging to sampling circuit, a pair of switching elements connected to the same signal line conduct simultaneously in response to signal line selection signal (See Fig. 3, items N-EN, Vdd1, in description See Col. 2, Lines 24-34).

It would have been obvious to one of ordinary skill in the art at the time of invention to use the groups of the switching elements belonging to sampling circuit, a pair of switching elements connected to the same signal line conduct simultaneously in response to signal line selection signal as shown by Jeong in the Proebsting, Akiyama et al. and Minami et al. apparatus in order to reduce power consumption.

As to claims 19-20, Proebsting, Akiyama et al. and Minami et al. do not show among the groups of the positive switching elements belonging to positive sampling circuit, a pair of switching elements connected to the same signal line conduct simultaneously in response to positive signal line selection signal and among the groups of the negative switching elements belonging to negative sampling circuit, a pair of switching elements connected to the same signal line conduct simultaneously in response to negative signal line selection signal.

Jeong teaches among the groups of the positive switching elements belonging to positive sampling circuit, a pair of switching elements connected to the same signal line conduct simultaneously in response to positive signal line selection signal and among the groups of the negative switching elements belonging to negative sampling

circuit, a pair of switching elements connected to the same signal line conduct simultaneously in response to negative signal line selection signal (See Figs. 1-3, items Channel, Row, N_EN, P_EN, OUTPUT, in description See from Col. 1, Line 16 to Col. 2, Line 34).

It would have been obvious to one of ordinary skill in the art at the time of invention to use the groups of the positive switching elements belonging to positive sampling circuit, a pair of switching elements connected to the same signal line conduct simultaneously in response to positive signal line selection signal and among the groups of the negative switching elements belonging to negative sampling circuit, a pair of switching elements connected to the same signal line conduct simultaneously in response to negative signal line selection signal as shown by Jeong in the Proebsting, Akiyama et al. and Minami et al. apparatus in order to reduce power consumption.

5. Claims 21-24, 45-48 are rejected under 35 U.S.C. 103(a) as being unpatentable over Proebsting, Akiyama et al. and Minami et al. as aforementioned in claims 2,4,8,10,41-44 in view Nakamura et al. (US Patent no. 6,411,273 B1)

Proebsting, Akiyama et al. and Minami et al. do not show switching elements are constituted of thin-film transistors.

Nakamura et al. teaches thin-film transistors as switching elements (See Fig. 14, items 117,117A, 118a, in description See Col. 45, Lines 11-16).

It would have been obvious to one of ordinary skill in the art at the time of invention to use thin-film transistors as shown by Nakamura et al. in the Proebsting,

Akiyama et al. and Minami et al. apparatus in order to reduce power consumption (See Col. 2, Lines 54-59 in Nakamura et al. reference).

Response to Amendment

6. Applicant's arguments filed on 02-12-04 with respect to claims 1-52 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

The Taguchi (US Patent No. 6, 191,779 B1) reference discloses LCD device and D/A converter.

The Hillis (US Patent No. 5, 212, 484) reference discloses two ADC, control and select logic.

The Ozguc (US Patent No. 5,689,259) reference discloses differential D/A converter with N-bits plus sign.

The Moriyama (US Patent No. 4,450,433) reference discloses D/A converting circuit having two D/A converters.

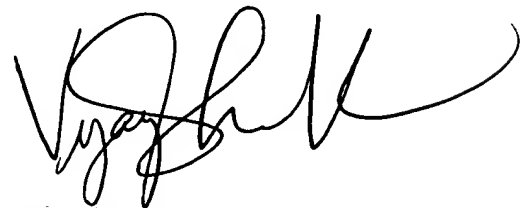
Telephone inquire

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Leonid Shapiro whose telephone number is 703-305-5661. The examiner can normally be reached on 8 a.m. to 5 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bipin Shalwala can be reached on 703-305-4938. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Is



VIJAY SHANKAR
PRIMARY EXAMINER